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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,119	07/15/2003	Thomas Wiegele	015559-288	7843

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EXAMINER	
WONG, TINA MEI SENG	
ART UNIT	**PAPER NUMBER**
2874	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,119	WIEGELE ET AL.	
	Examiner	Art Unit	
	Tina M. Wong	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28,31-56 and 113-130* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28,31-56 and 113-130* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 March 2006 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28, 31-56 and 113-130 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,525,864 to Gee et al.

In regards to claim 28, 31-33, 39 and 41, Gee et al discloses a wafer portion (Figure 5) including a microstructure (402) formed therein and located thereon and a solderable surface (501) configured to receive an electrical component, there the solderable surface is electrically and operatively coupled to the microstructure so that ii can control operate or receive inputs from at least part of the microstructure. Gee et al further discloses an upper wafer portion (410) coupled to a lower wafer portion (401) where the microstructure (402) is located on the upper wafer portion and the solderable surface (pad) is located on the lower wafer portion. Gee et al

further shows in Figure 5, the solderable surfaces are not positioned under the upper wafer portion and is exposed.

Although Gee et al does not explicitly state the upper or lower wafer portion to have a top view, it would have been obvious at the time the invention was made to a person having ordinary skill in the art that either the upper or lower wafer portion has a top view since the top view is dependant on the orientation of the device or the person. Therefore, the upper wafer portion would defines a coverage area in the top view and the solderable surface is not located within the coverage area, the upper wafer would include an outer perimeter where the outer perimeter defines the coverage area, and the lower wafer portion would have a coverage area in top view and wherein the coverage area of the upper wafer portion is entirely contained in the lower wafer portion.

In regards to claims 34-36, although Gee et al does not explicitly state the upper and lower wafer portions to be coupled together by a low temperature or photopatternable adhesive. However. Gee et al does not limit the coupling of the two wafer portions to soldering or flip-chip bonding techniques. Furthermore, the use of adhesives is widely used technique to bond wafers and substrates. Furthermore, when taking temperature/heat as a factor, the use of a low temperature adhesive would be preferable to prevent temperature from affecting other optical or electrical components. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used a low temperature or photopatternable adhesive.

In regards to claims 37, 40 and 123, Gee et al discloses the solderable surface to be a flip chip connection site configured to receiver a chip thereon by flip chip bonding.

In regards to claim 38, Gee et al discloses a plurality of conductive pads each electrically isolated from any adjacent pad. But Gee et al fails to disclose the conductive pads having a melting point of less than about 250°C. However, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have a melting point of less than about 250°C, since it has been held to be within the general skill of a worker in the art to select a known material or known characteristic on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416*

In regards to claims 42 and 49, Gee et al discloses a controller coupled to the solderable surface to cause and control the individual movement of each reflective surface.

In regards to claim 43, Gee et al discloses a microstructure with a sensor. Gee et al further discloses the mirrors to be actuated, so therefore, an actuator must also be present in the microstructure.

In regards to claim 44, Gee et al discloses a mirror array (410) including a plurality of movable reflective surfaces.

In regards to claim 45-47, Gee et al discloses at least two electrodes located below each of the reflective surfaces so that voltage applied across the electrodes and the reflective surfaces cause the reflective surfaces to move in at least two directions.

In regards to claim 48, Gee et al discloses the reflective surfaces to be individually controllable.

In regards to claim 50, although Gee et al disclose the size of the coverage area of the upper wafer to be smaller than the coverage area of the lower wafer.

In regards to claim 51, Gee et al discloses the reflective surfaces located on a layer. However, Gee et al fails to disclose the layer to be non-silicon. However, providing a reflective layer such as Gee et al discloses and Applicant claims would be advantageous. Although a non-silicon material is not specifically disclosed, Gee et al also does not limit the type of material that can be used as a reflective layer. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have provided a reflective coating.

In regards to claim 52, Gee et al fails to specifically disclose the reflective portions located on movable portions to be coupled to a base portion on the upper wafer. However, Gee et al does disclose the mirrors/reflective portions to tip when actuated and therefore, when tipped, the mirrors are rotated. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the moveable portions rotatably coupled to a base portion of the wafer.

In regards to claim 53, Gee et al discloses at least a portion of the upper wafer portion to be a SOI wafer.

In regards to claim 54, Gee et al discloses a wafer portion to be a ceramic substrate.

In regards to claim 55, Gee et al shows a lower wafer portion with an upper surface facing the upper wafer portion and the solderable surface located on the upper surface.

In regards to claim 56, Gee et al discloses a wafer portion with an upper portion and a lower portion including a microstructure formed therein and located thereon and a solderable surface configured to receive an electrical component, there the solderable surface is electrically and operatively coupled to the microstructure so that it can control operate or receive inputs from at least part of the microstructure. However, although Gee et al does not explicitly state the

upper or lower wafer portion to have a top view, it would have been obvious at the time the invention was made to a person having ordinary skill in the art that either the upper or lower wafer portion has a top view since the top view is dependant on the orientation of the device or the person. Therefore, the upper wafer portion would defines a coverage area in the top view. Additionally, although Gee et al does not explicitly state an electronic component not to be positioned under the wafer portion, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have an external electronic component to control the movement of the mirrors. By including an external electronic component, the manufacture of the micro system is greatly simplified.

In regards to claim 113, although Gee et al does not specifically disclose the upper and lower wafer portion to be coupled by an electrically insulating material, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have an electrically insulating material between the upper and lower wafer in order to prevent unwanted electrical signals from inadvertently passing between the two wafers.

In regards to claim 114, although Gee et al does not explicitly state an electronic component not to be positioned under the wafer portion, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have an external electronic component to control the movement of the mirrors. By including an external electronic component, the manufacture of the micro system is greatly simplified.

In regards to claim 115, Gee et al shows the electrical component to be positioned between the upper and lower wafer.

In regards to claim 116, Gee et al shows the entirety of the solderable surface to not be located within the coverage area.

In regards to claim 117, Gee et al shows the lower wafer portion having an upper surface facing the upper wafer portion where the solderable surface is located on the upper surface.

In regards to claim 118, Gee et al discloses an upper and lower wafer portion including a microstructure and at least one electrode for controlling the movement of at least part of the microstructure, a solderable surface located on the lower wafer portion and not located within a coverage area and an electronic component coupled to the solderable surface by flip chip bonding. But Gee et al fails to specifically disclose the electrode to be on the lower wafer portion. However, by including the drive structure and the linking framework as part of the lower wafer substrate, the electrode would be part of the lower wafer portion.

In regards to claim 119, although Gee et al does not specifically disclose the upper and lower wafer portion to be coupled by an electrically insulating material, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have an electrically insulating material between the upper and lower wafer in order to prevent unwanted electrical signals from inadvertently passing between the two wafers.

In regards to claim 120, although Gee et al does not specifically disclose the lower wafer portion to have a solderable surface located on the upper surface, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have placed a

solderable surface on the upper surface of the lower wafer portion in order to connect/join the lower wafer portion with the upper wafer portion in order for the system to communicate.

In regards to claim 121, Gee et al shows the electronic component to be located between the upper and lower wafer portion.

In regard to claim 122, Gee et al discloses an upper wafer portion including a microstructure, a lower wafer portion located below the upper wafer portion with at least one electrode for controlling the movement of the microstructure, a solderable surface located on the lower wafer portion and an electronic component coupled to the solderable surface. Additionally, Gee et al discloses an electronic component (drive circuit of the lower wafer portion) to be a separate component that is spaced apart from the electrode (406). Although Gee et al does not specifically disclose the electronic component and solderable surface to be located on the lower wafer portion, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the solderable surface and the electronic component located on the lower wafer portion since the lower wafer portion is provided as a substrate in order to support existing and additional components.

In regards to claims 129-130, Gee et al discloses a wafer portion including a microstructure formed therein and located thereon and a solderable surface configured to receive an electrical component, there the solderable surface is electrically and operatively coupled to the microstructure so that ii can control operate or receive inputs from at least part of the microstructure. Gee et al further discloses an upper wafer portion coupled to a lower wafer portion where the microstructure is located on the upper wafer portion and the solderable surface (pad) is located on the lower wafer portion. Gee et al further shows in Figure 5, the solderable

surfaces are not positioned under the upper wafer portion and is exposed. Although Gee et al does not specifically disclose the upper and lower wafer portion to be coupled by an electrically insulating material, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have an electrically insulating material between the upper and lower wafer in order to prevent unwanted electrical signals from inadvertently passing between the two wafers.

Furthermore, Gee et al does not explicitly state the upper or lower wafer portion to have a top view, however it would have been obvious at the time the invention was made to a person having ordinary skill in the art that either the upper or lower wafer portion has a top view since the top view is dependant on the orientation of the device or the person. Therefore, the upper wafer portion would defines a coverage area in the top view and the solderable surface is not located within the coverage area, the upper wafer would include an outer perimeter where the outer perimeter defines the coverage area, and the lower wafer portion would have a coverage area in top view and wherein the coverage area of the upper wafer portion is entirely contained in the lower wafer portion.

Response to Arguments

Applicant's arguments with respect to claims 28, 31-56 and 113-122 have been considered but are moot in view of the new ground(s) of rejection.

Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference B discusses a MEMS configuration of mirrors electrically controlled.

Inventorship

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tina M. Wong whose telephone number is (571) 272-2352. The examiner can normally be reached on Monday-Friday 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMW

SUNG PAK
PRIMARY EXAMINER